ABSTRACT OF THE DISCLOSURE

A receiver detects a highly precisely approximate value of the power of a reception signal with a high speed. A first comparator 11 compares a component I and component Q of a reception signal with each other to determine which one of these components is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value, a 3-bit shift register 12 multiplies the first output value by 1/8, a subtractor 13 subtracts the by-1/8-multiplied value from the first output value, a 1-bit shift register 14 multiplies the second output value by 1/2, a 2-bit shift register 15 multiplies the by-1/2-multiplied value by 1/4, a first adder 16 adds the first output value and the by-1/4-multiplied value, a second adder 17 adds an output value from the subtractor 13 and an output value from the 1-bit shift register 14, and a second comparator 18 compares the results of these two additions with each other to determine which one of these results is larger or smaller and output the value of a larger one thereof as an approximate value of the power of the reception signal.